Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A computerized ESD circuit design system, comprising:

a user interface for inputting a plurality of design parameters of a circuit;

an ESD kit comprising parameterized cells (p-cells) of low level electronic components and p-cells of higher level electronic circuit components, the higher level electronic circuit components comprising growable and non-growable segments; and

a circuit schematic module creating ESD elements for connection with the circuit based on the plurality of design parameters and using at least one of the low level electronic circuit components and higher level electronic circuit components.

[c2] 2. The computerized ESD circuit design system of claim 1, wherein the circuit schematic module places the ESD elements in the circuit.

[c3] 3. The computerized ESD circuit design system of claim 1, wherein said low level electronic components and

higher level electronic circuit components are in a hierarchical format.

[c4] 4. The computerized ESD circuit design system of claim 1, wherein the higher level electronic circuit components form repetition groups of an underlying p-cell element to accommodate different inputted design parameters when forming the ESD elements.

[c5] 5. The computerized ESD circuit design system of claim 1, wherein the p-cells of lower order electronic components fix some variables and pass some variables to the higher order p-cell electronic components through inheritance.

[c6] 6. The computerized ESD circuit design system of claim 1, further comprising a translation module for translating schematic representations of the ESD elements to graphical representations of the ESD elements and translating the graphical representations of the ESD elements to the schematic representations of the ESD elements.

[c7] 7. The computerized ESD circuit design system of claim 1, further comprising a library containing various types of the ESD elements.

[c8] 8. The computerized ESD circuit design system of claim 7, further comprising a module for manipulating the ESD

elements to conform with a design of the circuit.

[c9] 9. The computerized ESD circuit design system of claim 7, further comprising a pointer to the various types of the ESD elements in the library.

[c10] 10. The computerized ESD circuit design system of claim 7, wherein the various types of the ESD elements are preset or user designed.

[c11] 11. The computerized ESD circuit design system of claim 1, wherein the circuit schematic module creates one of a symbol and a schematic of the ESD elements.

[c12] 12. The computerized ESD circuit design system of claim 1, further comprising a graphical seed module for creating a graphical seed of at least the ESD elements and the circuit.

[c13] 13. The computerized ESD circuit design system of claim 12, wherein the graphical seed module includes functions of at least one of:

(i)Stretch,

(ii)Conditional Inclusion,

(iii)Repetition,

(iv)Parameterized shapes,

(v)Repeat along shape,

(vi)Reference point,

(vii)Inherited Parameters,

(viii)Parameterized Layer,

(ix)Parameterized Label,

(x)Parameterized Property,

(xi)Parameters, and

(xii)Compile.

[c14] 14. The computerized ESD circuit design system of claim 12, wherein the graphical seed module creates a graphical representation of the circuit and the designed ESD element for future fabrication.

[c15] 15. The computerized ESD circuit design system of claim 1, wherein the circuit schematic module creates a boundary about the ESD elements containing circuit information and places the schematic within the circuit design.

[c16] 16. The computerized ESD circuit design system of claim 1, further comprising a module for providing modification of ESD interconnect parameterized cells based on information of the higher level electronic circuit components.

[c17] 17. The computerized ESD circuit design system of claim 16, wherein said circuit schematic module provides a

static p-cell substantiation translator box used for comparison of the ESD interconnect parameterized cell and robustness of the ESD kit.

[c18] 18. The computerized ESD circuit design system of claim 16, further comprising a component to identify and verify a connection of at least one of a circuit type, the ESD interconnect parameterized cell, ESD type and a pad.

[c19] 19. The computerized ESD circuit design system of claim 1, further comprising:

a cell substantiation translator module for identifying which components is part of the higher level circuit elements;

a module for eliminating and preserving all of the higher level circuit elements in the cell substantiation translator module; and

a module for re-generation of all graphical information from the cell substantiation translator module based on the preserved higher level circuit elements for graphically representing the circuit and ESD elements.

[c20] 20. The computerized ESD circuit design system of claim 1, further comprising a component to establish an interconnection path of a pad level for an input pad and to

verify an ESD interconnect at the pad level.

[c21] 21. The computerized ESD circuit design system of claim 1, wherein a p-cell is established which prevents a metal level to go below a given ESD width where a minimum width is established by conversion of a metal shape into the p-cell where the metal has an algorithm with a minimum function where the width never goes below a given width defined by a minimum ESD requirement.

[c22] 22. A method of forming an electrostatic discharge (ESD) protection design, comprising the steps of:

forming a kit of parameterized cells (p-cells) modeling elements of an ESD protection device;

providing an input variable set;

providing a computer interface for allowing a user to input parameters for said input variable set;

forming a higher order ESD protection circuit from said p-cells based on said parameters; and

outputting said higher order ESD protection circuit in one of a circuit layout and a circuit schematic graphical format.

[c23] 23. The method of claim 22, further comprising the steps of:

forming a personalization and reduction of hierar-

chical form;

forming a interconnect p-cell;

providing a comparison of ESD robustness between said higher order ESD protection circuit and said interconnect p-cell; and

verifying ESD connectivity to pads.

[c24] 24. The method of claim 23, further comprising the step of defining a modification to ESD interconnects based on ESD robustness of said ESD protection device from its circuit type, size or inherited parameters.

[c25] 25. The method of claim 23, wherein a p-cell translator substantiation box provides mapping between said ESD protection circuit and said ESD interconnects.

[c26] 26. The method of forming claim 23, further comprising the step of checking correspondence established of the ESD circuit type and circuit function using the p-cell translator substantiation box.

[c27] 27. The method of claim 23, further comprising the step of establishing an interconnection path of a pad level for an input pad and verifying ESD interconnects at the pad level.

[c28] 28. The method of claim 27, further comprising the step

of verifying a connection of any of a circuit type, an ESD interconnect parameterized cell, ESD type and the input pad.

[c29] 29. The method of claim 23, further comprising the step of establishing an interconnection path of a pad level for the input pad and to verify an ESD interconnect at the pad level.

[c30] 30. The method of claim 22, further comprising the steps of:

identifying which components is part of the higher order circuit elements;

eliminating and preserving all of the higher order circuit elements; and

re-generating of all graphical information for graphically representing the circuit and ESD elements.

[c31] 31. A computer program product comprising a computer usable medium having readable program code embodied in the medium, the computer program product includes:

a component to verify a connection between a pad and an ESD network by verifying and checking electrical connectivity;

a component to verify the width requirements to

maintain ESD robustness to a minimum level;

a component to verify that based on the ESD robustness of the ESD network that the interconnect width and via number is such to avoid electrical interconnect failure prior to the ESD network failure;

a component to provide for multiple lines in parallel whose cross section can be maintained and evaluated as a set of parallel interconnect connected to a single ESD network or plurality of ESD networks;

a component to provide for "ESD ballasting" by dividing into a plurality of lines;

a component to provide for calculation of the ESD robustness of the interconnect based on pulse width, surrounding insulator materials, metal level and distance from the substrate;

a component to provide for surrounding fill shapes; and

a component to provide for and adjust for cheesing of the interconnect.